What is claimed is:

1. A method of forming a NAND memory array, the method comprising:

   forming a source slot and a drain contact region at opposite ends of a NAND string disposed on a substrate of the memory array using a single mask, the NAND string comprising a plurality of memory cells connected in series.

2. The method of claim 1, further comprising, before forming the source slot and the drain contact region, forming a dielectric layer on the substrate, the NAND string, and source and drain select gates respectively disposed at the opposite ends of the NAND string and electrically connected to the NAND string.

3. The method of claim 1, further comprising aligning the drain contact region to a sidewall of the drain select gate.

4. The method of claim 2, wherein forming the source slot and the drain contact region comprises removing the dielectric layer from the substrate.

5. The method of claim 1, further comprising forming a source line in the source slot and a drain contact in the drain contact region.

6. The method of claim 1, wherein the source slot and the drain contact region are formed substantially simultaneously.

7. The method of claim 5, further comprising forming a bit line contact in contact with the drain contact.

8. The method of claim 1, further comprising aligning the source slot to a sidewall of the source select gate.

9. A method of forming a NAND memory array, the method comprising:

forming a dielectric layer on a substrate, a NAND string disposed on the substrate, and source and drain select gates respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, the NAND string comprising a plurality of memory cells connected in series;

forming a bulk insulation layer on the dielectric layer; and

forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate.

10. The method of claim 9, wherein forming the source slot and the drain contact region comprises removing the dielectric layer from the substrate.

11. The method of claim 9, further comprising forming a source line in the source slot and a drain contact in the drain contact region.

12. The method of claim 11, further comprising forming a bit line contact in contact with the drain contact.

13. The method of claim 9, wherein the source slot is formed by self aligning the source slot to the dielectric layer on the source select gate.

14. The method of claim 9, wherein the dielectric layer is a nitride layer.

15. The method of claim 9, wherein the bulk insulation layer is of a doped silicate glass.

16. The method of claim 15, wherein the doped silicate glass is a borosilicate glass, phosphosilicate glass, or borophosphosilicate glass.

17. The method of claim 9, wherein self aligning the drain contact region to the dielectric layer on the drain select gate further comprises self aligning the drain contact region to another drain select gate connected to another NAND string.

18. A method of forming a NAND memory array, the method comprising:

forming a dielectric layer on a substrate, a NAND string disposed on the substrate, and source and drain select gates respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, the NAND string comprising a plurality of memory cells connected in series;

forming a bulk insulation layer on the dielectric layer;

forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain

contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate;

removing the dielectric layer from the substrate within the source slot and drain contact region;

forming a source line in the source slot and a drain contact in the drain contact region; and

forming a bit line contact in contact with the drain contact.

19. The method of claim 18, wherein forming the source line in the source slot and the drain contact in the drain contact region, comprises:

forming a polysilicon plug in the source slot in contact with the substrate and a polysilicon plug in the drain contact region in contact with the substrate; and

forming an electrically conducting plug on the polysilicon plug in the source slot and on the polysilicon plug in the drain contact region.

20. The method of claim 18, wherein the source slot is formed by self aligning the source slot to the dielectric layer on the source select gate.

21. The method of claim 18, further comprising forming an interlayer dielectric on the bulk insulation layer and on the source line and the drain contact before forming the bit line contact.

22. The method of claim 21, wherein the drain contact passes through the interlayer dielectric.

23. The method of claim 18, wherein the drain contact comprises a head connected substantially perpendicularly to a stem, wherein the bit line contact is formed in contact with the head.

24. The method of claim 23, wherein the head overlies the dielectric layer on the drain select gate and is aligned with the drain select gate, and the stem overlies the polysilicon plug.

25. A method of forming a NAND memory array, the method comprising:

forming a dielectric layer on a substrate, a NAND string disposed on the substrate, and source and drain select gates respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, the NAND string comprising a plurality of memory cells connected in series;

forming a bulk insulation layer on the dielectric layer;

forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate;

removing the dielectric layer from the substrate within the source slot and drain contact region;

forming a polysilicon plug in the source slot in contact with the substrate and a polysilicon plug in the drain contact region in contact with the substrate;

forming an electrically conducting plug on the polysilicon plug in the source slot and on the polysilicon plug in the drain contact region;

forming an interlayer dielectric on the bulk insulation layer, the electrically conducting plug in the source slot, and the electrically conducting plug in the drain contact region; and

forming a bit line contact through the interlayer dielectric in contact with the electrically conducting plug in the drain contact region.

26. The method of claim 25, wherein the source slot is formed by self aligning the source slot to the dielectric layer on the source select gate.

27. The method of claim 25, further comprising forming a metal layer on the interlayer dielectric in electrical contact with the bit line contact.

28. The method of claim 27, further comprising forming a bit line from the metal layer so that the bit line is in electrical contact with the bit line contact.

29. A NAND memory array comprising:

a substrate;

a source select gate formed on the substrate;

a drain select gate formed on the substrate;

a string of floating-gate memory cells formed on the substrate and connected in series between the source select gate and the drain select gate;

a drain contact comprising a head connected substantially perpendicularly to a stem, the head aligned with the drain select gate and overlying a dielectric layer formed on the drain select gate, the stem overlying a polysilicon plug formed on the substrate; and

a bit line contact in direct electrical contact with the head

30. The NAND memory array of claim 29, wherein the bit line contact is aligned with the drain select gate.

31. The NAND memory array of claim 29, wherein the bit line contact comprises a barrier layer disposed on the drain contact, a first metal layer disposed on the barrier layer, and a second metal layer disposed on the first metal layer.

32. The NAND memory array of claim 31, wherein the barrier layer, first metal layer, and second metal layer are respectively of titanium nitride, titanium, and tungsten.

33. The NAND memory array of claim 29, wherein the drain contact further comprises a barrier layer disposed on the polysilicon plug, a first metal layer disposed on the barrier layer, and a second metal layer disposed on the first metal layer.

34. The NAND memory array of claim 33, wherein the barrier layer, first metal layer, and second metal layer are respectively of titanium nitride, titanium, and tungsten.

35. The NAND memory array of claim 29, wherein

a source of the source select gate is coupled to a source line of the NAND memory array and a drain of the source select gate is coupled to a drain of a first floating-gate memory cell of the string of floating-gate memory cells;

a drain of the drain select gate is coupled to a bit line of the NAND memory array and a source of the drain select gate is coupled to a drain of a last floating-gate memory cell of the string of floating-gate memory cells; and

a control gate of each floating-gate memory cell is coupled to a word line of the NAND memory array.

36. A NAND memory device comprising:

an array of floating-gate memory cells, wherein the array comprises:

a plurality of rows of memory cells, each row coupled to a word line;

a plurality of columns of memory cells grouped in strings, each column coupled to a bit line, the memory cells of each string of memory cells connected in series between a source select gate and a drain select gate;

for at least one string of memory cells, a drain contact comprising a head connected substantially perpendicularly to a stem, the head aligned with a drain select gate and overlying a dielectric layer formed on that drain select gate, the stem overlying a polysilicon plug formed on a substrate of the memory device adjacent the drain select gate; and

a bit line contact coupled to the bit line and in direct electrical contact with the head.

37. The NAND memory device of claim 36, wherein the head of at least one drain contact is aligned with the drain select gate of its respective string of memory cells.

38. The NAND memory device of claim 36, wherein the head of at least one drain contact is aligned with the drain select gate of an adjacent string of memory cells.

39. An electronic system comprising:

a processor;

a NAND memory device coupled to the processor, the memory device comprising:

a substrate;

a source select gate formed on the substrate;

a drain select gate formed on the substrate;

a string of floating-gate memory cells formed on the substrate and connected in series between the source select gate and the drain select gate;

a drain contact comprising a head connected substantially perpendicularly to a stem, the head aligned with the drain select gate and overlying a dielectric layer formed on the drain select gate, the stem overlying a polysilicon plug formed on the substrate; and

a bit line contact in direct electrical contact with the head and aligned with the drain select gate.

40. The electronic system of claim 39, wherein

a source of the source select gate is coupled to a source line of the NAND memory device and a drain of the source select gate is coupled to a drain of a first floating-gate memory cell of the string of floating-gate memory cells;

a drain of the drain select gate is coupled to a bit line of the NAND memory device and a source of the drain select gate is coupled to a drain of a last floating-gate memory cell of the string of floating-gate memory cells; and

a control gate of each floating-gate memory cell is coupled to a word line of the NAND memory device.

41. An electronic system comprising:

a processor;

a NAND memory device coupled to the processor, the memory device comprising:

an array of floating-gate memory cells, wherein the array comprises:

a plurality of rows of memory cells, each row coupled to a word line;

a plurality of columns of memory cells, each column coupled to a bit line, the memory cells of each column connected in series between a source select gate and a drain select gate;

a drain contact comprising a head connected substantially perpendicularly to a stem, the head aligned with the drain select gate and overlying a dielectric layer formed on the drain select gate, the stem overlying a polysilicon plug formed on a substrate of the memory device adjacent the drain select gate; and

a bit line contact coupled to the bit line and in direct electrical contact with the head and aligned with the drain select gate.

42. A method of fabricating a portion of a memory device, comprising:

forming a plurality of serially-connected floating-gate transistors overlying a substrate, wherein the plurality of serially-connected floating-gate transistors form a NAND string;

forming a source select gate overlying the substrate and adjacent a source of a first floating-gate transistor of the plurality of serially-connected floating-gate transistors, a drain of the source select gate coupled to a source of the first floating-gate transistor;

forming a drain select gate overlying the substrate and adjacent a drain of a last floating-gate transistor of the plurality of serially-connected floating-gate transistors, a source of the drain select gate coupled to a drain of the last floating-gate transistor;

forming a first layer of dielectric material overlying the source select gate, the NAND string, the drain select gate, and exposed surfaces of the substrate adjacent the source and drain select gates;

forming a second layer of dielectric material overlying the first layer of dielectric material, wherein the second layer of dielectric material comprises a dielectric material different from the first layer of dielectric material;

patterning the second layer of dielectric material to expose portions of the first layer of dielectric material adjacent the source select gate, adjacent the drain select gate and overlying the drain select gate to thereby define a source slot and a drain contact region substantially concurrently;

removing exposed portions of the first layer of dielectric material adjacent the source select gate and adjacent the drain select gate, thereby exposing portions of the substrate adjacent the source select gate and the drain select gate;

forming a first layer of conductive material overlying the second layer of dielectric material and in contact with the exposed portions of the substrate;

removing an upper portion of the first layer of conductive material to recess it below a surface of the second layer of dielectric material, thereby leaving a first portion of the first layer of conductive material in the source slot and a second portion of the first layer of conductive material in the drain contact region;

substantially concurrently forming a source line coupled to the first portion of the first layer of conductive material and a drain contact coupled to the second portion of the first layer of conductive material;

forming a third layer of dielectric material overlying the second layer of dielectric material, the source line, and the drain contact; and

forming a bit line contact through the third layer of dielectric material and coupled to a portion of the drain contact overlying the drain select gate.

43. The method of claim 42, wherein the first layer of dielectric material is formed from tetraethylorthosilicate.

44. The method of claim 42, wherein the second layer of dielectric material is formed from a doped silicate glass.

45. The method of claim 44, wherein the doped silicate glass is a borosilicate glass, phosphosilicate glass, or borophosphosilicate glass.

46. The method of claim 42, wherein the first layer of conductive material is polysilicon.

47. The method of claim 42, wherein forming the source line and the drain contact comprises respectively forming barrier layers on the first and second portions of the first layer of conductive material, respectively forming first metal layers on the barrier layers, and respectively forming second metal layers on the first metal layers.

48. The method of claim 47, wherein the barrier layers, first metal layers, and second metal layers are respectively of titanium nitride, titanium, and tungsten.

49. The method of claim 42, further comprising patterning the third dielectric layer and etching through the third dielectric layer before forming the bit line contact.

50. The method of claim 49, further comprising forming a barrier layer on the drain contact, a first metal layer on the barrier layer, and a second metal layer on the first metal layer to form the bit line contact.

51. The method of claim 50, wherein the barrier layer, first metal layer, and second metal layer are respectively of titanium nitride, titanium, and tungsten.

52. The method of claim 42, wherein the third layer of dielectric material is selected from the group consisting of silicon oxides, silicon nitrides, and silicon oxynitrides.

53. The method of claim 42, further comprising forming a second layer of conductive material overlying the third layer of dielectric material and in contact with the bit line contact.

54. The method of claim 53, further comprising forming a bit line from the second layer of conductive material so that the bit line is in contact with the bit line contact.

55. The method of claim 54, wherein forming the bit line comprises patterning and etching the second layer of conductive material.

56. The method of claim 42, further comprising aligning the drain contact region to a sidewall of the drain select gate.

57. The method of claim 42, further comprising aligning the source slot to a sidewall of the source select gate.

58. The method of claim 42, wherein patterning the second layer of dielectric material further comprises forming a single mask layer on the second layer of dielectric material.

59. The method of claim 42, further comprising etching through the exposed portions of the first layer of dielectric material adjacent the source select gate, adjacent the drain select gate and overlying the drain select gate to form the source slot and the drain contact region.

60. The method of claim 59, wherein etching is carried out using at least one of carbon trifluoride, carbon tetrafluoride, and difluoromethane with argon.

61. The method of claim 42, wherein removing the exposed portions of the first layer of dielectric material adjacent the source select gate and adjacent the drain select gate comprises etching through the exposed portions of the first layer of dielectric material.

62. The method of claim 61 wherein etching is carried out using at least one of carbon trifluoride and carbon tetrafluoride.